Design & Analysis of Low Voltage A/D Converter Based Latched Comparator Using 0.18µm Technology.

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Abstract— Analog-to-Digital conversion process is an electronic process in which an analog signal is changed, without changing its necessary contents, into a digital signal. Latched comparators use positive feedback mechanism (aids in the input signal) to re-generates (amplifies) the analog input signal into a full scale digital level output signal. This paper presents the analysis of conventional comparator and latched comparator. The proposed design will improve the comparator performance by reducing the propagation delay and power consumption**.**The analysis and simulation results are obtained in 0.18µm with supply voltages of 1.8V respectively. The schematic of comparator is captured using EDA tool.

Index Terms— Operational Amplifier, CMOS, Design, 2-stage Comparator, Conventional Comparator, Latched Comparator, Low power consumption.

1 INTRODUCTION

A Comparator is a circuit that compares an analog signal with another analog signal or reference & outputs a binary signal based on comparison. The comparator is widely used in process of converting analog signals into digital signals. In the A/D conversion process, it is necessary to first sample the input. This sampled signal is than applied to a combination of comparators to determine the digital equivalent of the analog signal [1] and it compare the analog signal with another reference signal and outputs are binary signal based on the comparison. Low power consumption is an important feature of many A to D converters especially those used in portable devices that have limited power supply energy. A common technique to reduce its power is the adoption of a latch comparator design. Latch comparator can solve the power problem by removing the pre-amplifying stage [2], while achieving a smaller area. This paper focuses on charge sharing comparator as it combines the advantages of both, resistive dividing comparator & differential current sensing comparator.

2 COMPARATOR

2.1 Comparator Operation

The comparator senses the charge imbalance produced by the input at the preamplifier and reacts to that imbalance to create desired digital voltage levels at the output. In this manner this comparator can also be called a current comparator.

The whole operation of comparison is divided into two phases of the clock. In the first phase when the clock is high, the switch transistor closes and short-circuits both the outputs of the comparator and set them to certain DC voltage level around midpoint of VDD. In the same phase the pre-amplifier creates charge imbalance at the differential nodes of the latch. In the second phase, the pre-amplifier is disconnected from the comparator and the short-circuiting transistor is also switched off. Now the comparator (or the inverter pair) amplifies the charge imbalance into digital voltage levels on the differential nodes [5].

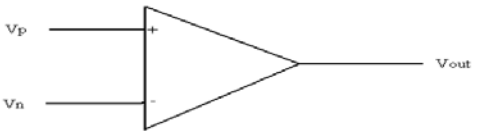

Fig.1. Comparator Symbol.

The output of comparator is high (VDD) when the difference between the non inverting and inverting input is positive, and low (VSS) when this difference is negative.

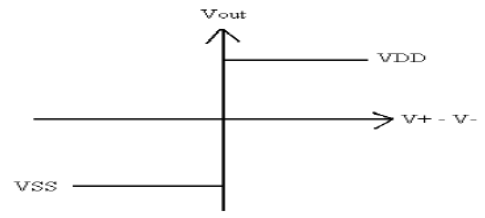

Fig.2. Output of Comparator.

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The comparator is a critical part of almost all kind of analog-to-digital (ADC) converters [8]. Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of the target application.

2.2 Specific Regenerative Structure

The following parameters were taken into consideration before finalizing the specific chosen architecture for the latch.

- Speed: A comparator with only two inverters connected to each other in a closed loop makes the regenerative structure very fast. Primarily because of the simplicity of the circuit as only 4 (two NMOS - PMOS pair) transistors are used in the inverter combination. This reduces the parasitic capacitance and hence comparison speed can be achieved.
- Rail-to-Rail output: As in most of the other designs of the latches, there is always a biasing transistor connected to the source of the NMOS in the regenerative loop. This raises the V_{OL} for the latch and hence minimum value close to the VSS cannot be achieved. In this chosen architecture, the biasing transistor is eliminated and self biasing techniques are used to attain required voltage levels and therefore rail to rail output is closely achieved.
- Reset: During the reset phase, the switching transistor short circuits the latch's outputs and the output is set to a point approximately equal to 1/2 VDD. The advantage for this characteristic feature is that in the second phase the regenerative loop can easily shift the output to the corresponding digital levels as determined by the charge imbalance. This also increases the speed and performance of the comparator. In other comparator designs, the latch is usually set to a floating state in the reset mode, so then chances of correct evaluation decreases as the outputs are not short-circuited to same DC level. This leads to a memory effect in the latch.

3 Designing of Comparator

3.1 Conventional Comparator Design

The design of comparator is similar enough to that of an op-amp [7]. An Op-Amp can be characterized by high input impedance, high gain margin, low output impedance, high band width. It has also the ability to amplify the differential mode signal to a high extent and attenuates or rejects the common mode signal. For op-amp design the multi-stage topology, especially more than two stages, the stability will increase. In order to obtain a high enough gain, two fully differential auxiliary operational amplifiers act like a booster. Hence, we'll depict the two stage topology method for the amplifier design [11].

The circuit in fig. 3. consists of a cascode of Voltage to Current and Current to voltage stages. First stage consists of a differential amplifier of NMOS transistor (M1, M2) converting the differential input voltage to differential currents. Which are applied to a current mirror load of PMOS transistor (M3, M4) recovering the voltage [11]. The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. C_L is the load capacitor and C_c is the compensation capacitor required for stability.

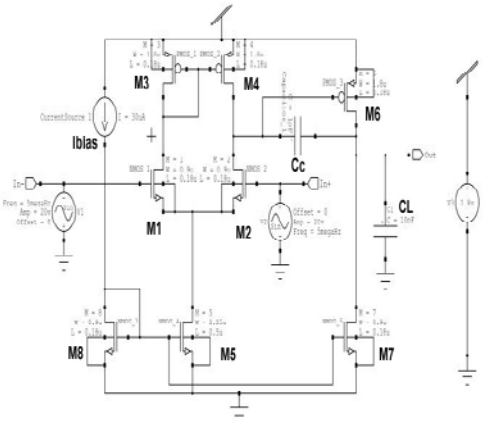

Fig. 3. Topology of op-amp design choosen.

Specifications:
Supply VDD=1.8V
Gain >65db
Gain Band Width =10MHz
Slew Rate =50V/µs
Input Common Mode Range= 0.4-3V
CL =1PF

The only difference is the use of the compensation network consists of resistor and capacitor and extra multipliers on a biasing NMOS device. The comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed as it will only slow down the switching speed. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail [3].

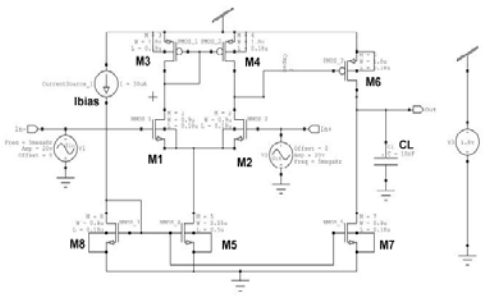

Fig.4. Schematic Design of Comparator.

In fig. 4, comparator consists of 8 transistors. The n-channel

transistors *M*1 and *M*2 form the input differential pair, and the p-channel transistors *M*3 and *M*4 form the active load. The diff-amp input stage is biased by the current mirror *M*5 and *M*6, in which the reference current is supplied by Ibias . The second stage, which is also the output stage, consists of the common-source connected transistor *M*7. Transistor *M*8 provides the bias current for *M*7 and acts as the active load.

3.1 Latched Comparator Design

The comparator [4] uses the regenerative structure of a dynamic latch. It consists of two inverters connected back to back with each other forming a differential comparator and an NMOS transistor is connected between the two differential nodes of the latch.

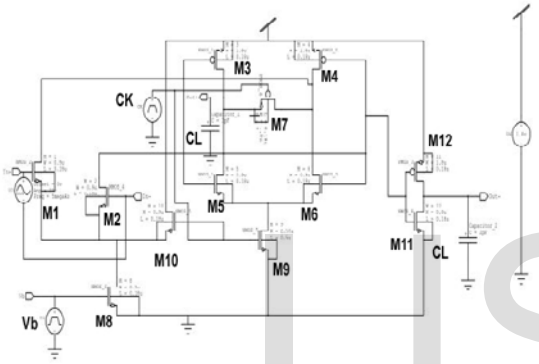

Fig.5. Schematic Design of Latched Comparator.

The latched comparator shown in fig.5 produces rail-to-rail logic level and consumes low power [6]. In this comparator, the pull-up is not as fast, hence, it operates at lower speed. Due to the low power consumption, rail-to-rail output swing and comparatively high speed of operation, the latched comparator shown in figure 5 has been selected. This latched comparator consists of a differential pair M1-M2 and a latch pair M5-M6, both sharing the cross coupled load M3-M4. There are two operating phases of this latched comparator: tracking phase and latching phase. During the tracking phase, the clock signal "CK" is low making transistor M9 "off" which prevents any current flow through M5-M6. Also, in this phase the equalization transistor switch M7 turns "on" which along with M3-M4 forms the load to the differential pair M1-M2. In the latching phase, the clock signal "CK" becomes high turning "off" M7 and turning "on" M9. This makes M3-M5 and M4-M6 as two back-to-back CMOS inverters that regenerate the small output voltage to full-scale digital levels.

4 Result

The results of conventional comparator and latched comparator are found by using t-spice code and output by w-edit of Tanner EDA tool and implemented by using 0.18um CMOS Technology. Input sine wave frequency up to 5MHz. Supply Voltage= ±1.8V.

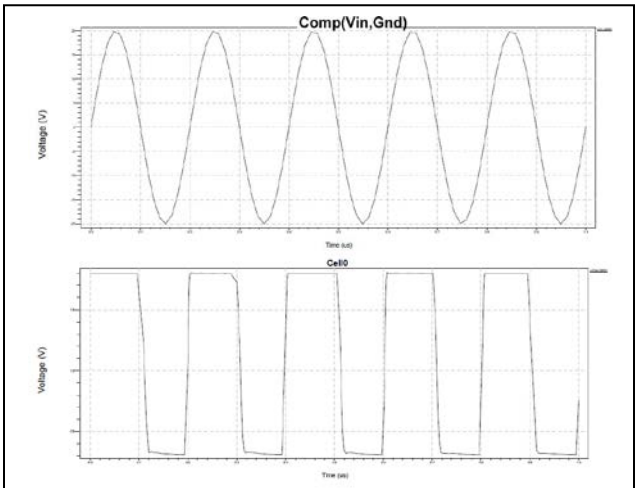

Fig.6. Output of Conventional Comparator.

The shorter propagation delay, the higher the speed of the circuit and vice-versa. Delay time is measured at 90% transition of the point. The propagation delay is determined using two basic time intervals, which is T_{PHL} and T_{PLH}. T_{PLH} is the delay time measured when output is changing from logic 0 to logic 1 and T_{PHL} is from logic 1 to 0. The total propagation delay for 2-stage conventional comparator comes out to be 2.8830e-009 seconds and power consumption is 9.2733e-006 Watt.

For Latched comparators designing the parameters taken are:

TABLE 1
MAIN DESIGN PARAMETERS

Parameters	Value
Voltage input (Vin)	1.8v
Voltage reference (Vref)	0.9v
All MOS Transistor length	0.18 μm
PMOS width	1.8 μm
NMOS width	0.9 μm

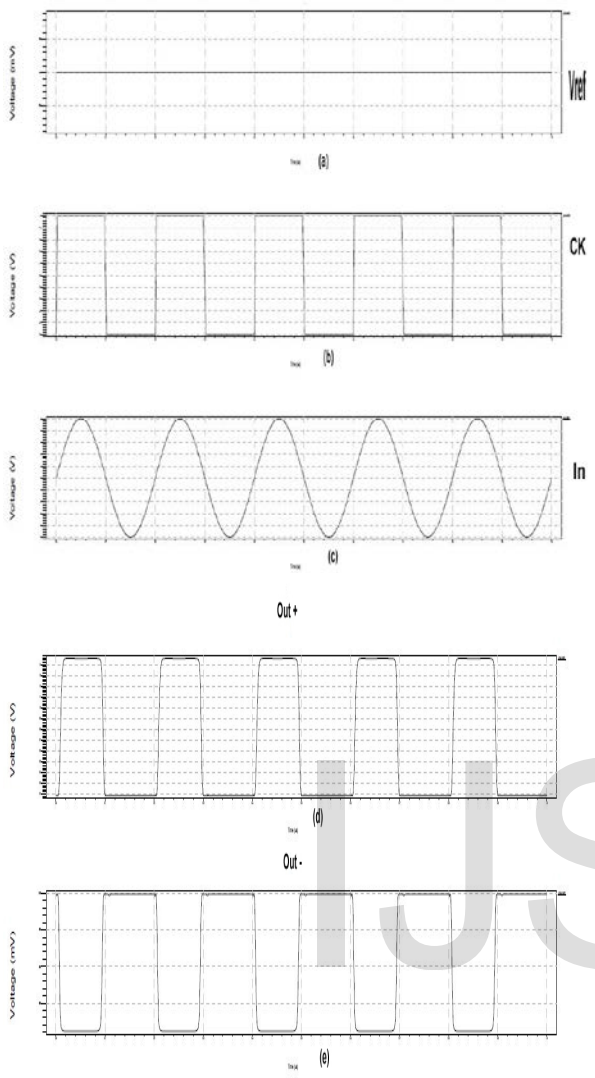

Fig.7. Transient analysis of Latched Comparator.

In the fig. 7, waveform 7(a) shows the Vref and waveform 7(b) shows the clock signal applied, waveform 7(c) shows the analog input. Waveform 7(d) and 7(e) shows the output at Out+ and Out- of latched comparator in fig. 6 .

The overall propagation delay of the above circuit (Fig. 5) comes out to be 1.23e-009 seconds and power consumption is 1.05446e-006 Watt.

The transient analysis of reference [10] is given in fig. 8. With comparison to reference paper [10], the output obtained is better and gives less propagation delay. Table 2 presents the comparison between the proposed work and previous work comparator.

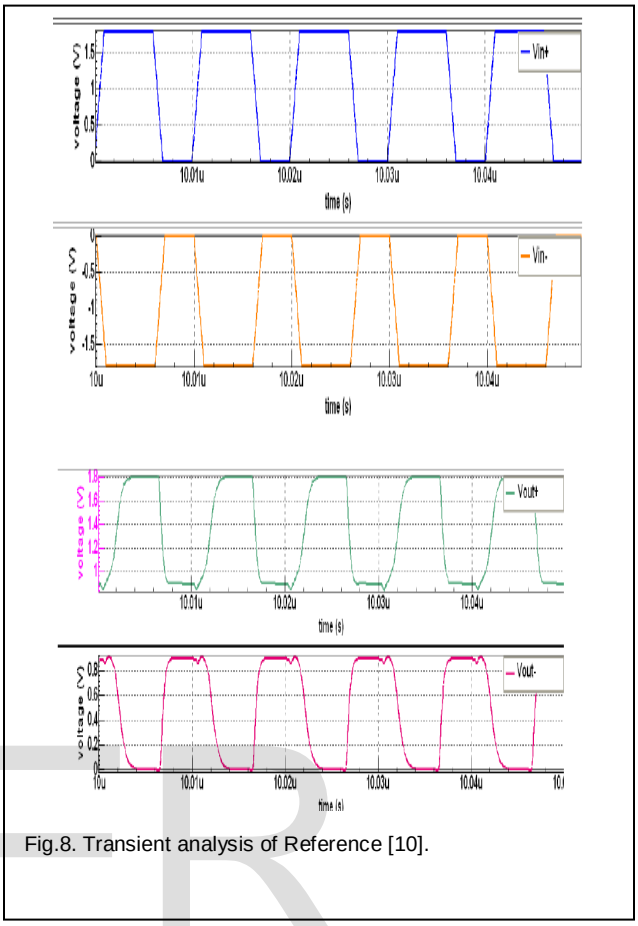

Fig.8. Transient analysis of Reference [10].

TABLE 2

PERFORMANCE COMPARITION OF COMPARATORS

	Reference[9]	Reference[10]	Present work
Length	0.5µm	0.18µm	0.18µm
W_p / W_n	10µm/5µm	8µm/4µm	1.8µm /0.9µm
Voltage supply	3.3V	1.8V	1.8V
Delay	1.827ns	1.54ns	1.23ns

Above comparison table describe that the proposed work gives the lowest delay. So now Table 3 shows the comparison of proposed comparator with the 2 stage comparator.

TABLE 3
COMPARITION TABLE

	Conventional comparator	Latched comparator
Technology	0.18µm	0.18µm
Voltage supply	1.8V	1.8V
Delay	2.88ns	1.23ns
Power Consumption	9.27µWatt	1.05µWatt

The Total Propagation Delay of the latched comparator comes out to be 1.23ns which is less than delay of 2-stage Comparator having a delay of 2.88ns. So the Latched Comparator shows reduced delay and hence it will show better speed as compared to the conventional comparators. The latched comparator's power consumption is 1.05µWatt which is also less than 2-stage comparator having power consumes 9.27µWatt.

4 CONCLUSION

The comparative analysis of Conventional 2-stage comparator with Latched comparator gives result that with the same input specifications, the delay as well as the power consumption is less in case of latched comparator. Hence, the latched comparator shows better speed with less power consumption. So, simulation results confirm that the proposed design procedure can be utilized to design that meet all the required specifications. The design is on 0.18µm technology. The total power consumed is 1.05µW which is better and effective one to design an ADC for application.

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